

PATENT APPLN. NO. 10/501,522
RESPONSE UNDER 37 C.F.R. §1.111

**PATENT
NON-FINAL**

IN THE CLAIMS:

1. - 15. (Canceled).

16. (Previously presented) A bonded SOI substrate comprising:
a SOI layer in which a device is to be formed; and
a supporting substrate wafer for supporting said SOI layer,
said SOI layer and said supporting substrate wafer having been
bonded to each other with an insulation layer interposed
therebetween, in which

said insulation layer has a plurality of cavities defined by
different heights.

17. (Previously presented) A bonded SOI substrate in
accordance with claim 16, said bonded SOI substrate comprising:

a SOI layer in which a device is to be formed; and
a supporting substrate wafer for supporting said SOI layer,
said SOI layer and said supporting substrate wafer having been
bonded to each other with an insulation layer interposed
therebetween, in which

said SOI layer has varied thickness over a plane thereof.

PATENT APPLN. NO. 10/501,522
RESPONSE UNDER 37 C.F.R. §1.111

**PATENT
NON-FINAL**

18. (Previously presented) A manufacturing method of a bonded SOI substrate, comprising:

a recessed portion forming step for forming a recessed portion in a surface of an active layer wafer and/or in a surface of a supporting substrate wafer;

a bonding step for bonding said active layer wafer and said supporting substrate wafer to each other with said surface(s) having said recessed portion(s) formed therein serving as bonding surface(s) to thereby form a cavity; and

a thinning step for thinning said active layer wafer of said bonded wafers to thereby form a SOI layer, wherein

in said recessed portion forming step, a plurality of recessed portions having varied depth is formed in said surface of said active layer wafer and/or in said surface of said supporting substrate wafer.

19. (Previously presented) A manufacturing method of a bonded SOI substrate in accordance with claim 18, in which in said bonding step, an insulation film has been formed on said bonding surface of said active layer wafer and/or on said bonding surface of said supporting substrate wafer.

PATENT APPLN. NO. 10/501,522
RESPONSE UNDER 37 C.F.R. §1.111

**PATENT
NON-FINAL**

20. (Previously presented) A manufacturing method of a bonded SOI substrate in accordance with claim 18, in which said bonding step is carried out in a vacuum atmosphere or under a vacuum condition.

21. (Previously presented) A manufacturing method of a bonded SOI substrate in accordance with claim 18, in which said thinning step includes a step for grinding and polishing of said active layer wafer after having been bonded together.

22. (Previously presented) A manufacturing method of a bonded SOI substrate in accordance with claim 18, further comprising a step for performing an ion implantation to a location in a specified depth in said active layer wafer, wherein

said thinning step includes, in the course of a heat treatment following to said bonding step, a step for separating a surface side of said active layer wafer from said ion-implanted region.

23. (Currently amended) A semiconductor device comprising a bonded SOI substrate in which a SOI layer having varied thickness is formed over a plane thereof and a cavity is formed at the bonding interface between said SOI layer and said substrate,

PATENT APPLN. NO. 10/501,522
RESPONSE UNDER 37 C.F.R. §1.111

PATENT
NON-FINAL

wherein a functional block defined by a CMOS logic is formed in the thinnest region of said SOI layer and a memory functional block and/or an analog block are formed in the other regions of said SOI layer.

24. (Previously presented) A semiconductor device in accordance with claim 23, in which a basic unit block of the CMOS logic is formed in the thinnest region of said SOI layer.

25. (Previously presented) A semiconductor device in accordance with claim 24, in which a unit transistor is formed in the thinnest region of said SOI layer.

26. (Previously presented) A semiconductor device in accordance with claim 25, in which a channel of a unit transistor is formed in the thinnest region of said SOI layer.